# B.Tech I Year

Regular Course Handbook

**Subject Name: Fund. Of Electronics Engineering (Unit-2)**

B.Tech First Year: Regular Course Lecture Plan Session 2022-23

| Subject Name | FUNDAMENTALS OF ELECTRONICS ENGINEERING |
|---|---|

| Unit No. | Unit Name | Syllabus Topics | Lecture No |
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| 1 | Semiconductor Diode, Diode Application & Special Purpose two terminal Devices | Introduction of Semiconductors: Intrinsic & Extrinsic Semiconductors, Types of currents, Movement of electrons & holes etc. | 1 |
| | | Working of semiconductor diode in no bias, forward bias conditions & reverse bias condition | 2 |
| | | Explanation of diode equation, V/I characteristics of pn junction diode, Analysis of effect of temperature on different parameters of diode | 3 |
| | | Problems based on diode equation and temperature effect, Illustration of ideal and simplified circuit representation of diode based on approximations | 4 |
| | | Problems based on series & parallel circuits of diodes | 5 |
| | | Explanation of two breakdown conditions under reverse bias conditions, Zener diode As Shunt voltage regulator | 6 |
| | | Problems based on voltage regulator | 7 |
| | | Working of Half wave and Full wave rectifiers | 8 |
| | | Different parameters of rectifiers and comparison between rectifiers on basis of these parameters | 9. |
| | | Numericals based on rectifiers | 10 |
| | | Different types of clampers and steps to draw their waveforms, Problems based on clampers | 11 |
| | | Voltage multiplier | 12 |
| | | Clippers: Introduction,types and problems | 13 |
| | | Special Purpose diodes | 14 |
| 2 | Bipolar Junction Transistor and Field Effect Transistor | Illustration of meaning of word transistor, its classification, introduction of structure of BJT, Explanation of current flow in BJT, Conditions for different regions of operation and their uses | 15 |
| | | Introduction of CB Configurations of BJT: Structure, Current gain, Input Characteristics, Output Characteristics | 16 |
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| | | Use of JFET as VVR, Different parameters of JFET. Introduction of DMOSFET, Output and Transfer. | 20 |
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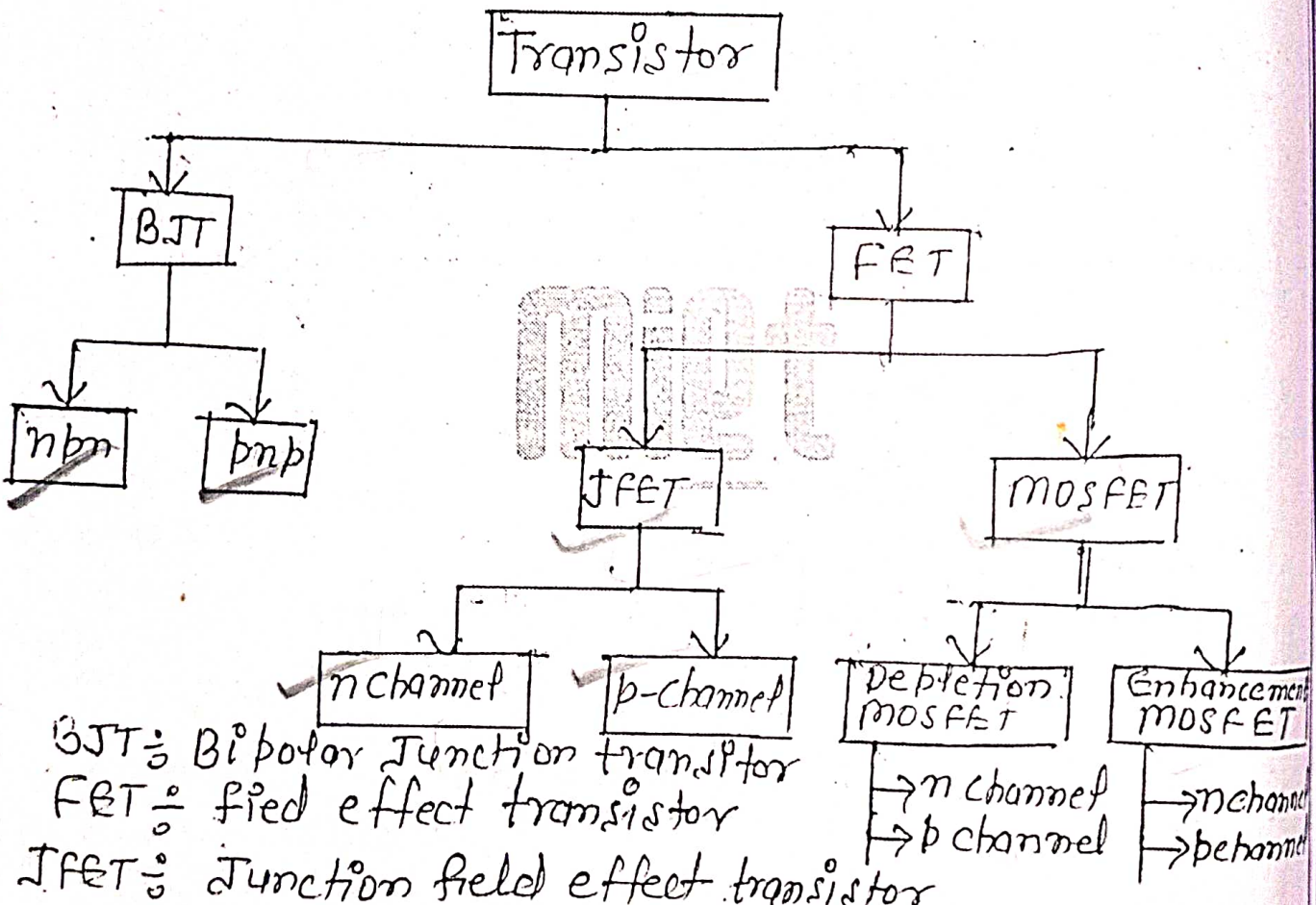
Transistor :- Transistor is a device which transfer applied signal from one type of resistor to other type of resistor. For example signal can be transferred from low resistor to high or from high resistor to low.

('Transistor') ⇒ Transfer + resistor

Classification of transistor :-

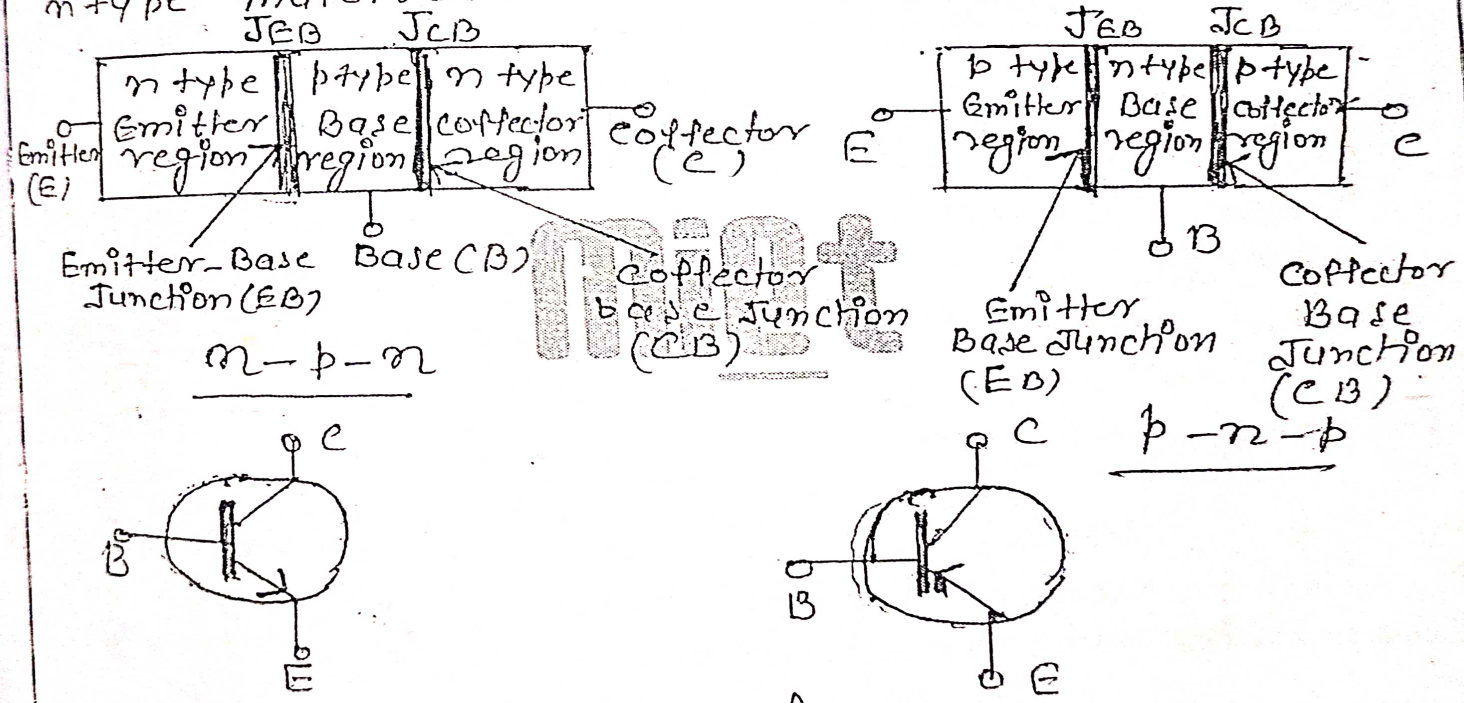



BJT :- Bipolar Junction transistor
FET :- fied effect transistor
JFET :- Junction field effect transistor
MOSFET :- metal oxide semiconductor field effect transistor.

Ques 1 ⁰/₀ Discuss the construction doping profile and physical appearance of Emitter, base and collector of a transistor. (2020-21, 2015-16 2013-14)

Ans ⁰/₀ construction of transistor (BJT) ⁰/₀

BJT consist of a layer of n type material sandwiched between two p type materials or one p type material is sandwiched between two n type materials.




Symbol

Emitter ⁰/₀ It is the highest doping region in the transistor. It supplies (emits) carrier to the base. It supplies electron to the base in n-p-n and holes in p-n-p.

Base :- The middle part of transistor is called base. It is very thin and lightly doped. So most of the carrier coming from emitter passes to collector.

Collector :- Collector collects the carrier which are coming from base. Doping of collector is heavier than base but less than emitter.

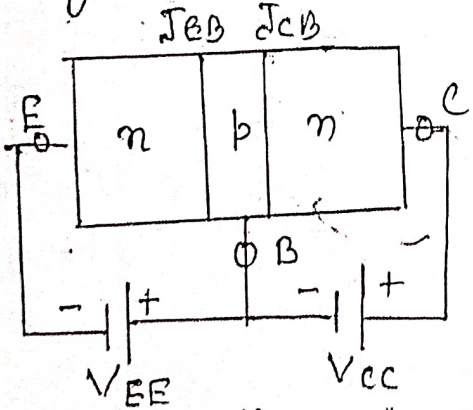
Area profile : C > E > B

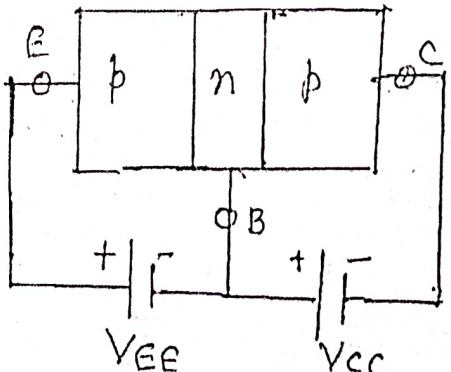
Doping profile : E > C > B

Ques 2:- Discuss different mode or working regions of BJT.

Ans :- BJT operates in three modes.

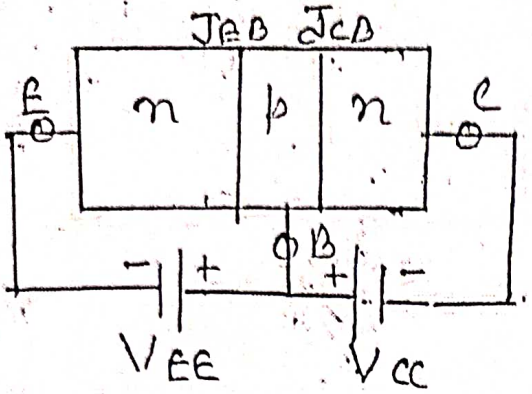
i) Active region :- In active region emitter-base junction ($J_{EB}$) is forward biased and collector-base junction ($J_{CB}$) is reverse biased. In this region BJT works as an amplifier.

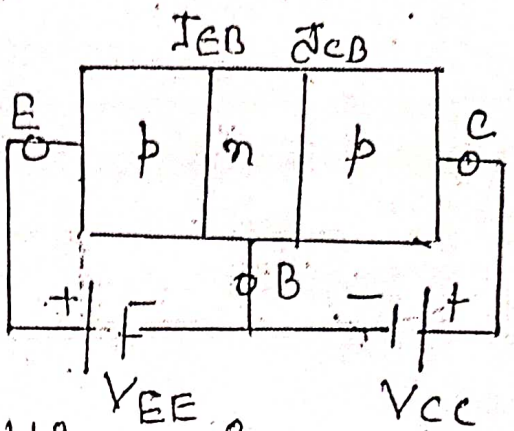


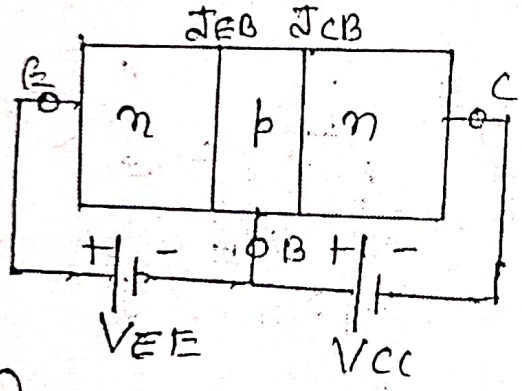

(ii) Saturation region :- In this region emitter-base junction ($J_{E-B}$) is forward biased and collector-base junction ($J_{CB}$) is forward biased. In this region BJT

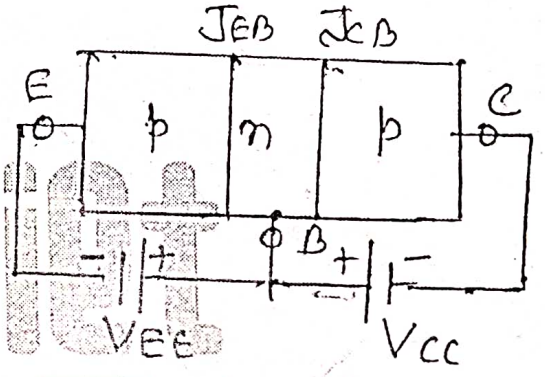
works as a closed switch.




(iii) Cut off region :- In this region emitter-base junction ($J_{EB}$) and collector base junction ($J_{CB}$) are reverse biased. In this region transistor (BJT) works as a open switch.



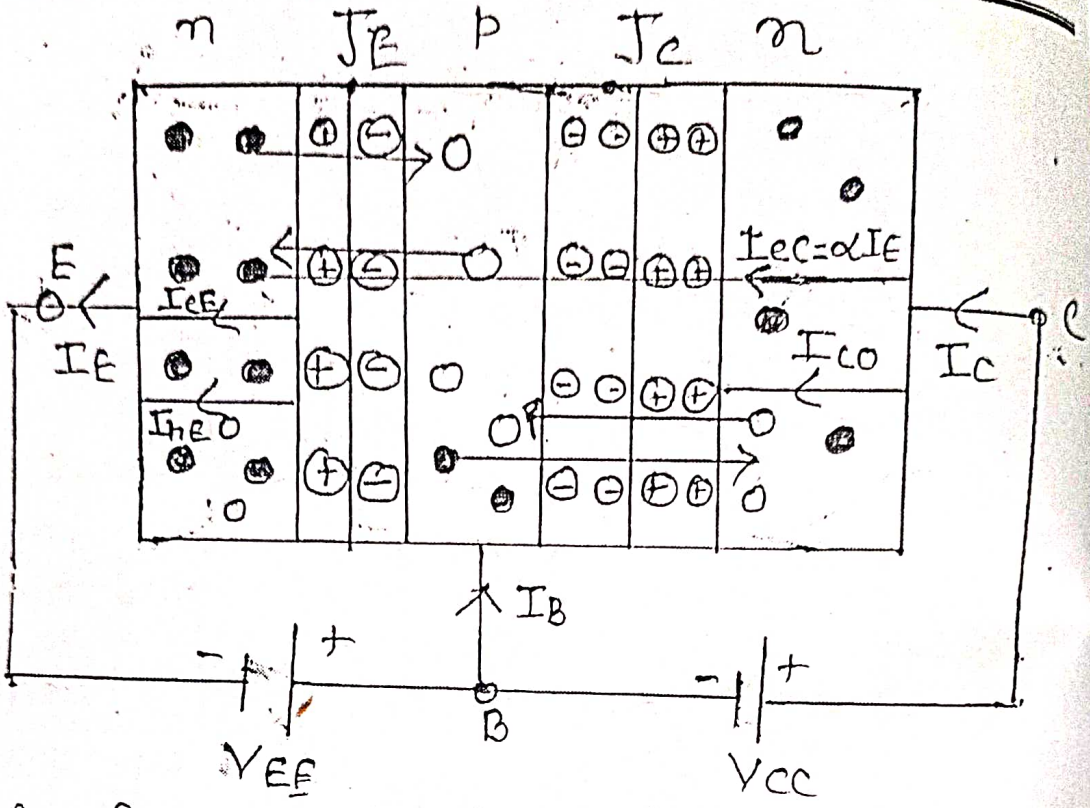




Ques 3 :- Explain the operation of n-p-n transistor in active region.

Or

Explain various current components in n-p-n transistor with the help of suitable diagram (2016-17)

Ans :- For active region Emitter base Junction ($J_{EB}$) must be forward biased and collector base junction ($J_{CB}$) must be reverse biased.




JE is forward biased by battery VEE .. so depletion layer will decrease and majority carrie flows from emitter to base giving current IE.

IE has two components.

$$I_E = I_{eE} + I_{hB} \quad ---- 1$$

- IeE : current due to electrons of emitter re
- IhB : current due to holes in base region

Since holes are majority carrier in emitter so,

$$I_{eE} \gg I_{hB}$$

So eqn 1 becomes $\boxed{I_E = I_{eE}}$ ---- 2

In base region there is recombination betwee electron and holes due to which base current is obtained. As number of holes in base are ver small so, base current is very small.

JC is reverse biased by Vc So collector current is due to flow of mino carriers from both side of the function

So collector current is given by

$$I_C = I_e\alpha + I_{CO}$$

But $I_{eC} = \alpha I_E$

$$\boxed{I_C = \alpha I_E + I_{CO}}$$

And

$$\boxed{I_E = I_B + I_C}$$

where $\alpha$ is transportation factor or current gain of BJT

Ques :- 4 :- Why BJT is called bipolar device?

Ans :- BJT is called bipolar device because its operation depends on both majority and minority carrier.

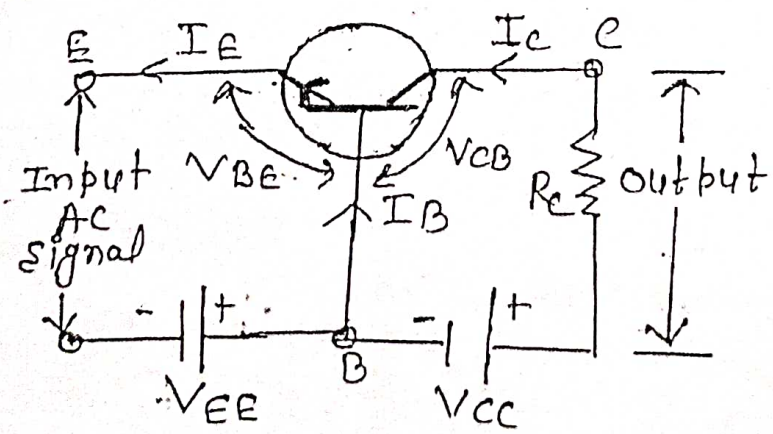
Transistor configuration or Connection :-

- Transistor has three terminals emitter, base and collector. But we require four terminals to connect the transistor in a circuit as an amplifier. Two for input and two for output.
- This is acheived by making one terminal of transistor common to input and output.
- So, transistor has three configurations based on common terminal.

i) Common base configuration (CB)
ii) Common emitter configuration (CE)
iii) common collector configuration (CC)

Ques :- 1 Explain the working of common base circuit with its circuit diagram. (2015-16)

Ans :- In common base input is applied between emitter and base. output is taken out from collector and base. So base is common between input and output.



i) DC current gain($\alpha_G$): It is the ratio of output current ($I_C$) to the input current ($I_E$)

$$\alpha = \frac{I_C}{I_E}$$

Since $I_E > I_C$ so value of $\alpha$ is less than 1. value of $\alpha$ ranges from .90 to .99. So no current gain is available in CB configuration.

ii) Expression for output current :-

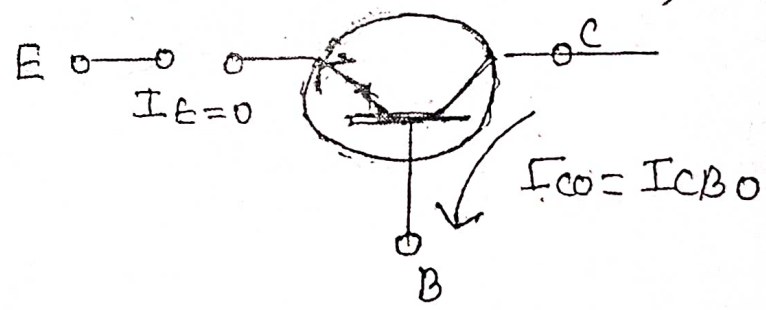
$$I_C = I_{eE} + I_{CO}$$

but $I_{eE} = \alpha I_E$

$$I_C = \alpha I_E + I_{CO}$$

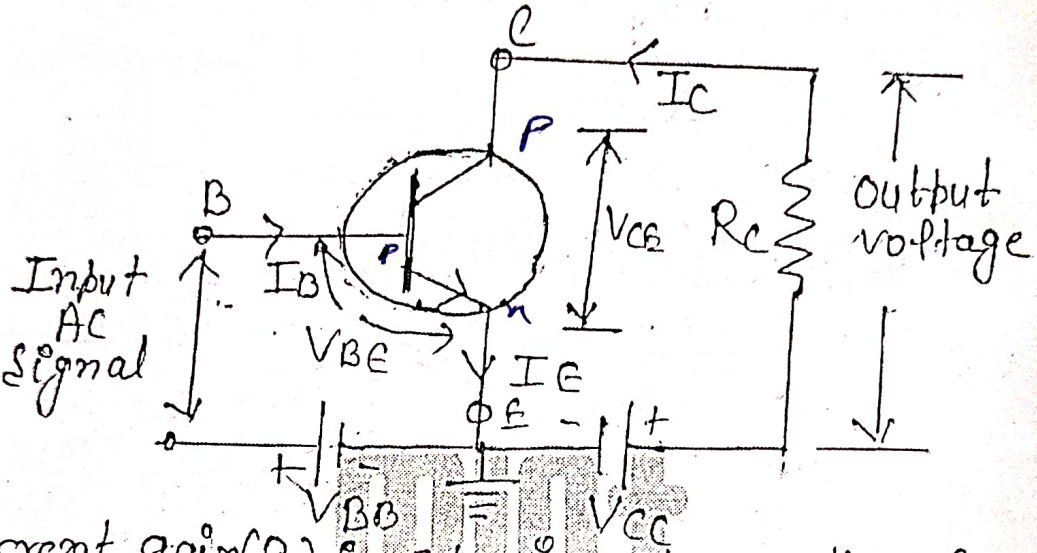
for CB $I_C = I_{CBO}$, $I_E = 0$

(Reverse leakage current between collector and base while emitter is open i.e. $I_E = 0$)



Ques:- 2 :- Explain the working of common emitter circuit. (2016-17, 2015-16)

Ans:- In CE configuration input is applied between base and emitter while output is taken out from collector and emitter. So, emitter of transistor is common to both input and output.




i) DC current gain ($\beta$) is the ratio of output current ($I_C$) to the input current ($I_B$).

$$\beta = \frac{I_C}{I_B}$$

Since value of $I_B << I_C$. So $\beta >> 1$. So current gain is available in CE configuration. Value of $\beta$ varies from 20 to 500.

(ii) Expression for output current :-

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha (I_C + I_B) + I_{CBO} \quad (I_E = I_C + I_B)$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \quad \text{---} 1$$

but $\beta = \frac{\alpha}{1-\alpha}$

$$\frac{\alpha}{1-\alpha} + 1 = \beta + 1$$

$$\frac{1}{1-\alpha} = \beta + 1 \quad \text{---- 2}$$

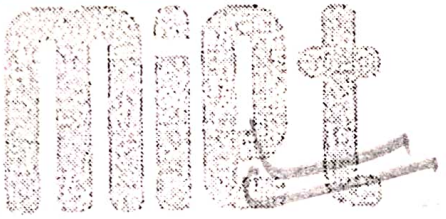
using eqn (1) and (2)

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

where $I_{CEO}$ : leakage current between collector and emitter while base is open i.e. $I_B = 0$

$$\boxed{I_{CEO} = (\beta + 1) I_{CBO}}$$



$$\boxed{I_C = \beta I_B + I_{CEO} - CE}$$

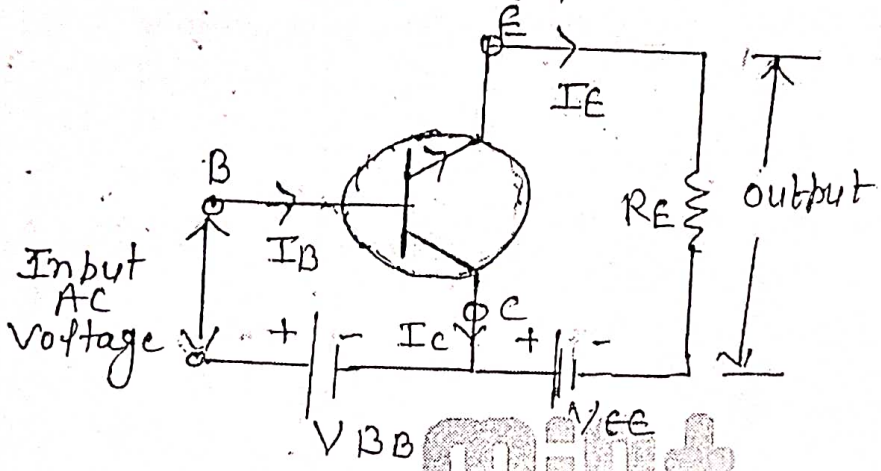
$$I_C = \alpha I_E + I_{CO} \rightarrow CB$$

$$I_C = I_{CBO}$$

$$\boxed{I_{CEO} = (\beta + 1) I_{CBO}}$$

Ques:- 1 Explain the common collector configuration in case of n-p-n transistor. (2015-16)

Ans:- In CC configuration input is applied between base and collector while output is taken out from emitter and collector. So, collector of transistor is common to both input and output.




i) DC current gain:- It is the ratio of output current ($I_E$) to the input current ($I_B$).

$$\gamma = \frac{I_E}{I_B}$$

Since value of $I_B << I_E$. So $\gamma > 1$. Therefore current gain is available in CC configuration. But voltage gain is not available in CC.

ii) Expression for output current:-

$$I_E = I_B + I_C$$

$$= I_B + \alpha I_E + I_{CBO}$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

But $\gamma = \frac{1}{1-\alpha}$

V. Imp

$$\boxed{\text{So } I_E = \gamma I_B + \gamma I_{CBO}}$$

Ques 2 Derive the relation between $\alpha$, $\beta$, and $\gamma$.

Ans We know that

$$\alpha = \frac{I_C}{I_E} \quad \text{and} \quad \beta = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C$$

Dividing both sides by $I_C$

$$\frac{I_E}{I_C} = \frac{I_B + I_C}{I_C}$$

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta} \Rightarrow \alpha + \alpha\beta = \beta$$

$$\beta(1-\alpha) = \alpha$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Now $I_E = I_B + I_C$

Dividing both sides by $I_B$

$$\frac{I_E}{I_B} = \frac{I_B}{I_B} + \frac{I_C}{I_B}$$

$$\boxed{\gamma = \beta + 1}$$

$$\gamma = \frac{\alpha}{1-\alpha} + 1$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

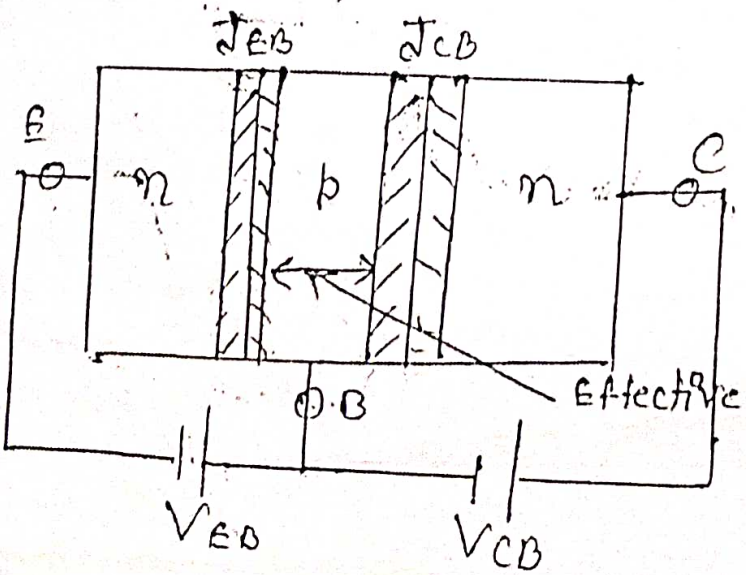
Ques ÷ 2 what is base width modulation (early effect.) (2011-12)

Ans ⁰₀ Base width modulation ⁰₀

- In active region $J_{EB}$ is forward biased and $J_{CB}$ is reverse biased. Also doping profile is $D_E > D_C > D_B$
- So width of depletion layer formed on E_B junction and C_B junction is non uniform. At both the junction major width of depletion is towards the base. So effective width of base is very small.

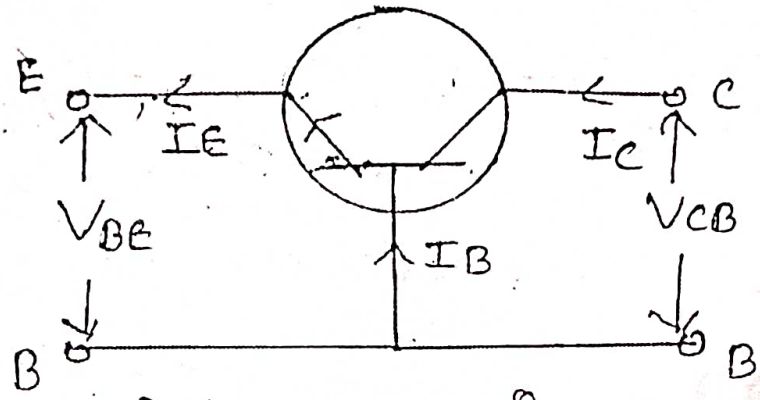
On increasing $V_{CB}$ effective width of base region further reduces. This effect is called base width modulation or early effect.

- on increasing $V_{CE}$ $I_E$ and $I_C$ increases but $I_B$ decreases (Due to reduction in base width, possibility of recombination in this region reduces)
- Thus $\alpha, \beta, \gamma$ increases.

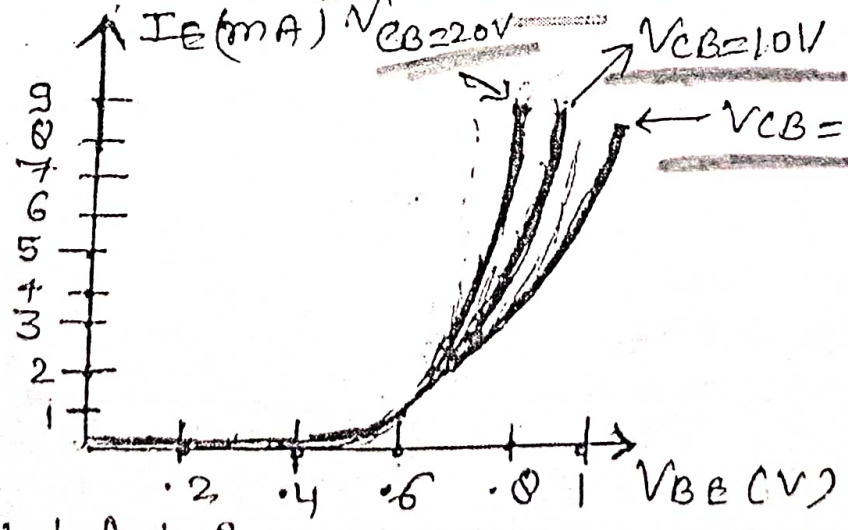


**Ques 1:** Draw the I/P and o/p characteristics of common base (CB) configuration. (2011-12, 2015-16)

**Ans:**



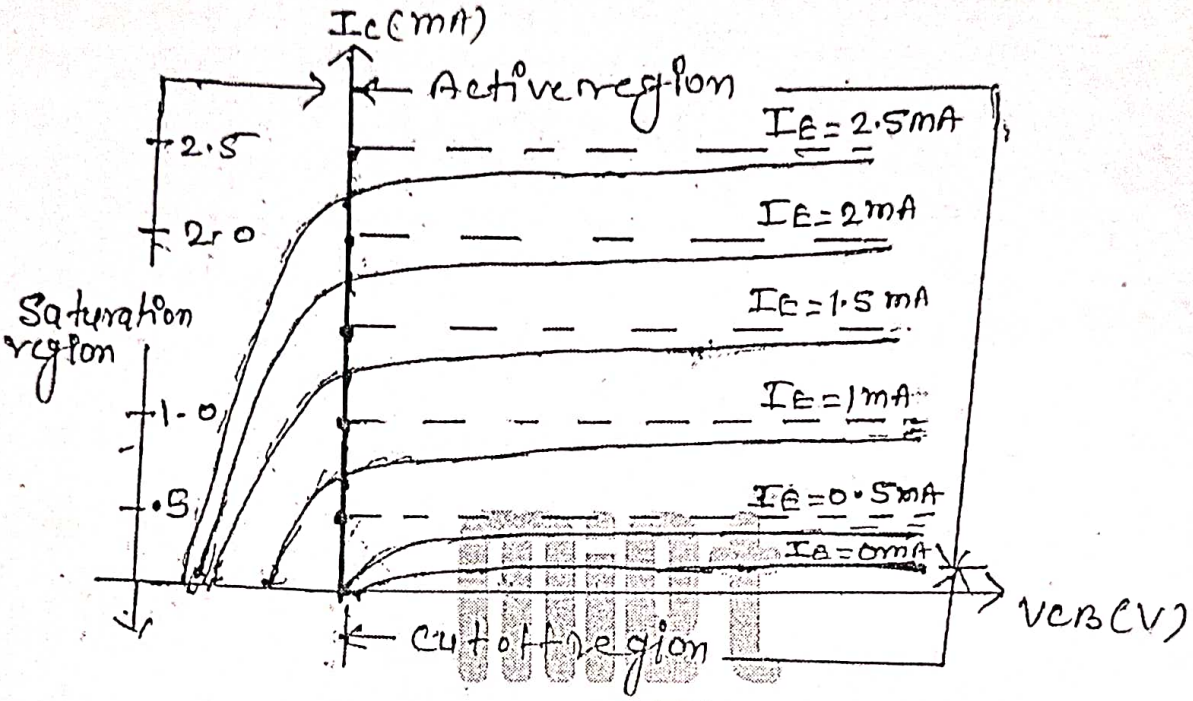

**Input Characteristics:** It is the graph between input current and input voltage for a constant output voltage. In CB configuration input current is $I_E$ and input voltage is $V_{BE}$ while output voltage is $V_{CB}$.




Important point:

- Input characteristics is identical to the V-I characteristics of forward biased diode.
- As $V_{CB}$ increases $I_E$ increases slightly due to early effect.

**Output Characteristics :-** It is the graph between output current and output voltage for constant input current. In CB output current is $I_C$ and output voltage is $V_{CB}$ while input current is $I_E$.




**Active region :-** For given $\alpha$ and $I_E$, $I_C$ is dependent only on $I_{CBO}$ which is slightly deband on $V_{CB}$. So graph of active region is almost constant.

$$I_C = \alpha I_E + I_{CBO}$$

**Saturation region :-** When the transistor is switched from active to saturation region, a large change in collector current for very small value of forward bias voltage at collector to base junction is obtained in negative direction.

**Cut-off region :-** When both the junction are reverse bigsed a very small collector current is obtained which is close to horizontal line.

$I_C = \alpha I_E + I_{CBO}$

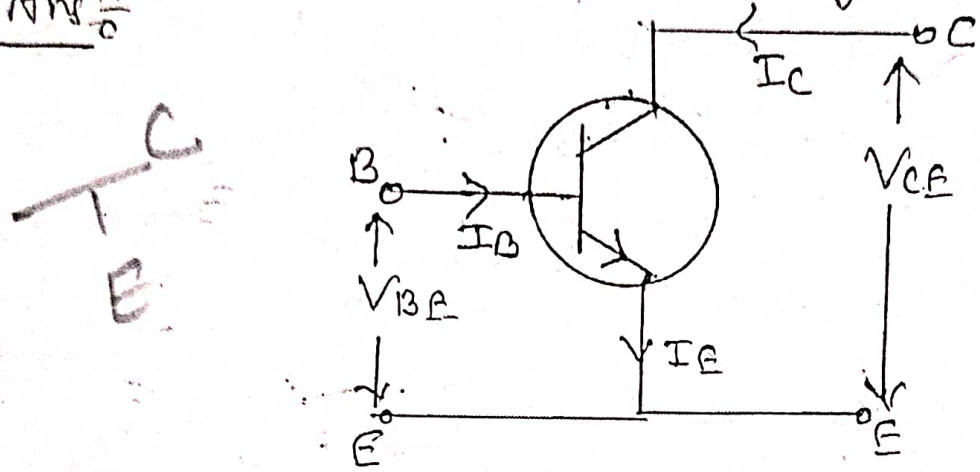
In cut-off region $I_E = 0$

Then $I_C = I_{CBO}$

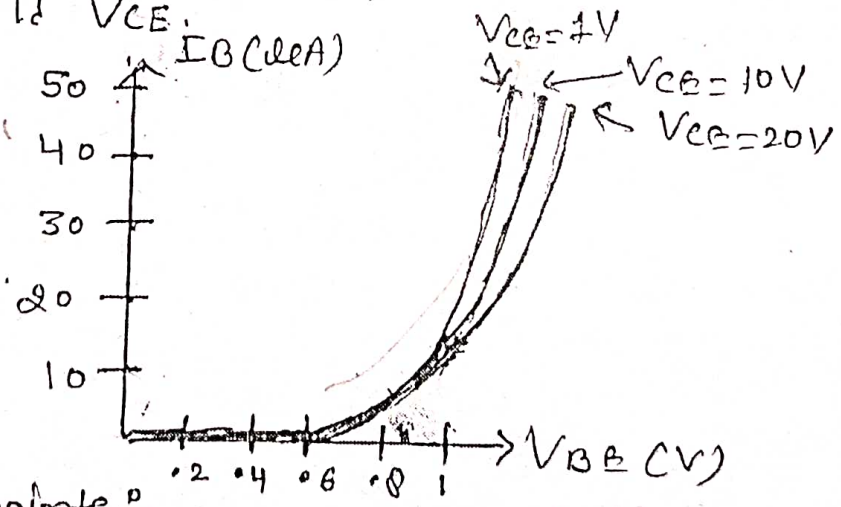
V. Imp

**Ques 2** Draw the I/P and O/P characteristics of common emitter configuration. (2010-11, 2011-12, 2015-16, 2020-21)

**Ans**



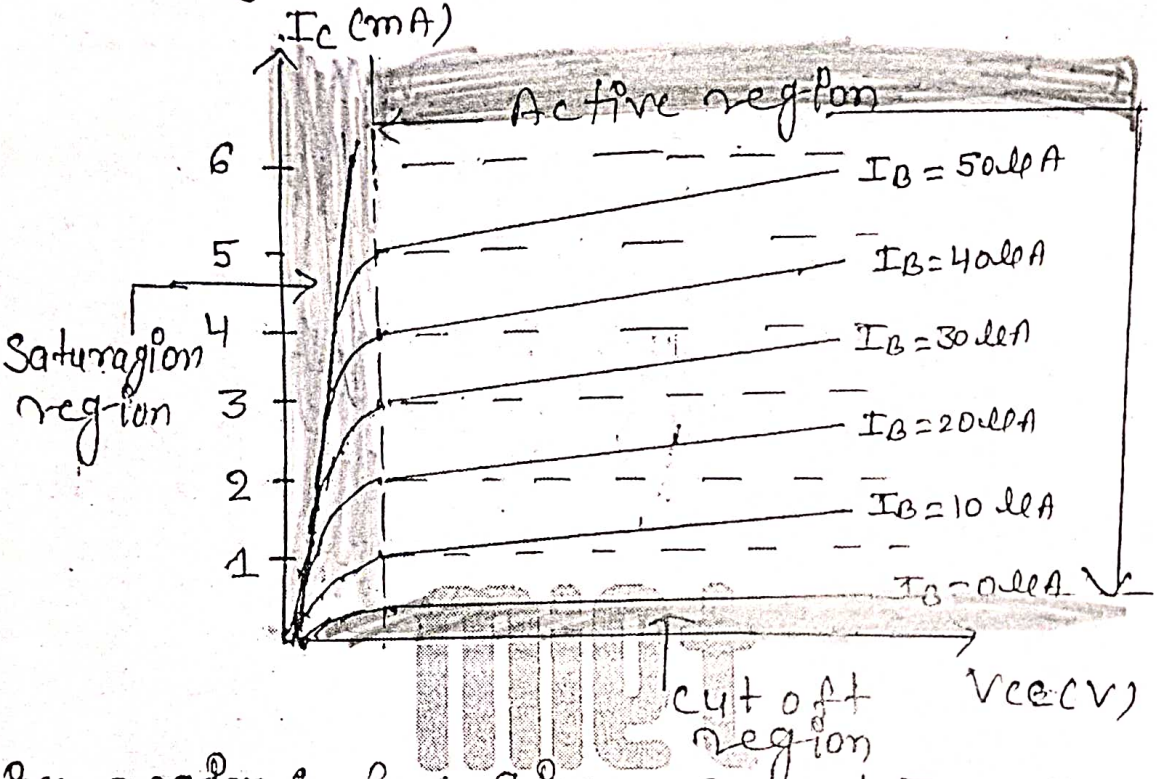

**Input characteristics** It is the graph between input current and input voltage for a constant output voltage. In CE input current is $I_B$ and input voltage is $V_{BE}$ while output voltage is $V_{CE}$.




Important points

- Input characteristics is identical to the V-I characteristics of forward biased p-n junction diode.
- As $V_{CE}$ increases $I_B$ decreases slightly due to early effect.

Output characteristics:- It is a graph between output current and output voltage for constant input current. For CB output current is $I_C$ and output voltage is $V_{CB}$ while input current is $I_E$.




- Active region:- For given $\beta$ and $I_B$, $I_C$ is dependent on $(\beta+1) I_{CBO}$ which is more dependent on $V_{CE}$ than the case in CB. So graph of active region has some slope showing change in $I_C$ on changing in $V_{CE}$

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

- Saturation region:- When the transistor is switched from active region to saturation region a large change in collector current for very small change in collector voltage is obtained in negative direction.
- cut-off region:- When both junction are reverse biased a very small collector current is obtained which is close to horizontal axix. $I_C = \beta I_B + (\beta+1) I_{CBO}$

In cutoff region $I_B = 0$

Then $I_C = (\beta+1) I_{CBO}$

Ques:- 1 Compare different configuration of BJT.

Ans:-

| S.N. | Characteristics | Common Base | Common Emitter | Common Collector |
|---|---|---|---|---|
| 1. | Input resistance | Low (about 100Ω) | Low (about 750Ω) | Very high (about 750kΩ) |
| 2. | Output resistance | Very high (about 450kΩ) | High (about 45kΩ) | Low (about 50Ω) |
| 3. | Voltage gain | high (about 150) | Very high (about 500) | No gain (less than 1) |
| 4. | Curren gain | No (less than 1) | high | Very high |
| 5. | Application | For high frequency application | For audio frequency application | For Impedance matching |

Ques2:- Why BJT is called current controlled device. (2017-10)

Ans:- BJT is called current controlled device because output is controlled by input current. In B.J.T the base current controls the current flow from emitter to Collector.

Ques:-3- In n-p-n transistor with $\beta = 98$ is operated in the CB configuration. If the emitter current is 2mA and reverse saturation

current is 12.6 nA. what are the base and collector current? (2016-17)

Soln :- given: $\beta = 98$, $I_E = 2mA$, $I_{CBO} = 12.6nA$

$$\alpha = \frac{\beta}{1+\beta} = \frac{98}{1+98} = .989$$

For CB. $I_C = \alpha I_E + I_{CBO}$

$= .989 \times 2 \times 10^{-3} + 12 \times 10^{-6}$

$= 1.99\ mA$

$I_E = I_C + I_B$

$I_B = I_E - I_C = 2.00 - 1.99 = .01\ mA$

Ques :- 4 A transistor having $\alpha = 0.975$ and $I_{CO} = 10\mu A$ is operated in CE mode. what is $\beta$ for the configuration. If the $I_B$ is $250\mu A$ then calculate $I_E$ & $I_C$. (2013-14)

Ans :- given $\alpha = 0.975$, $I_B = 2.50\mu A$, $I_{CO} = I_{CEO} = 10\mu A$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.975}{1-0.975} = \frac{.975}{0.025} = 39$$

Now for CE

$I_C = \beta I_B + I_{CEO}$

$= 39 \times 250 \times 10^{-6} + 10 \times 10^{-6}$

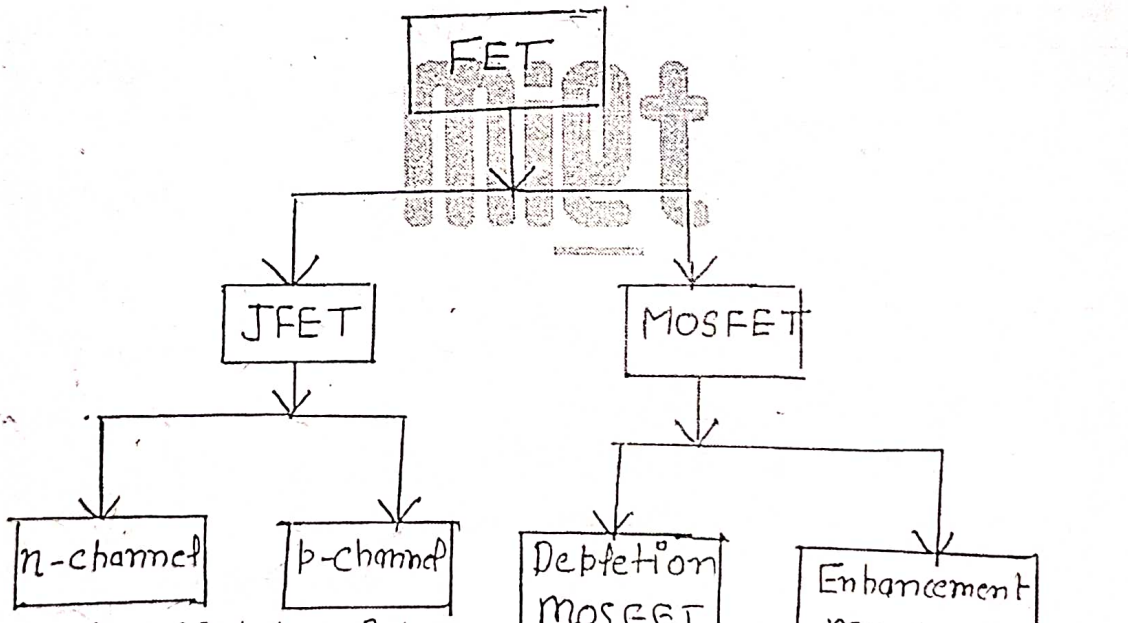
$= 9.76\ mA$

$I_E = I_C + I_B$

$= 9.76 + 0.25$

$= 10.01\ mA$

- The BJT has two principal disadvantage:
  i) It has low input impedance due to forward biased emitter junction.
  ii) It has considerable noise level.
- the above mentioned problems are overcomed by field effect transistor (FET).
  - The FET has large input impedance by virtue of its construction and biasing.
  - The FET is generally much less noisy than bipolar transistor.
- Classification of FET :-

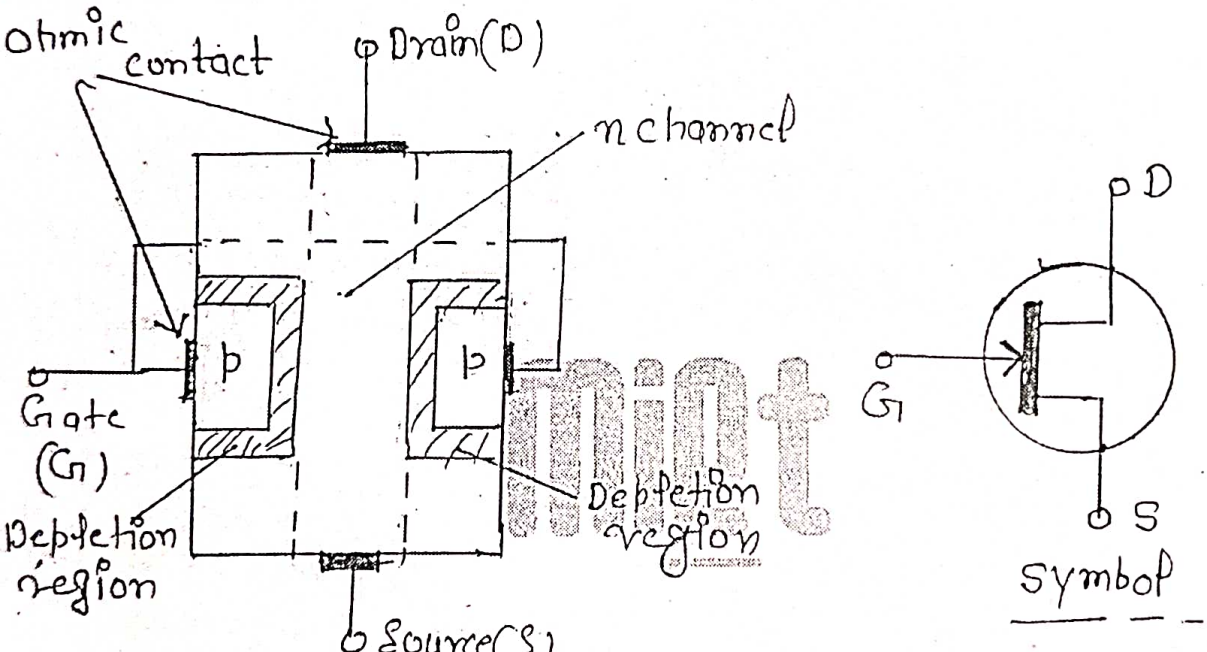



FET: Field effect transistor
JFET: Junction field effect transistor
MOSFET: Metal Oxide semi-conductor field effect transistor

Very Imp

**Ques:-1** Explain the construction and working of N-channel JFET. Draw the drain characteristics and transfer curves. (2015-16, 2016-17, 2017-18).

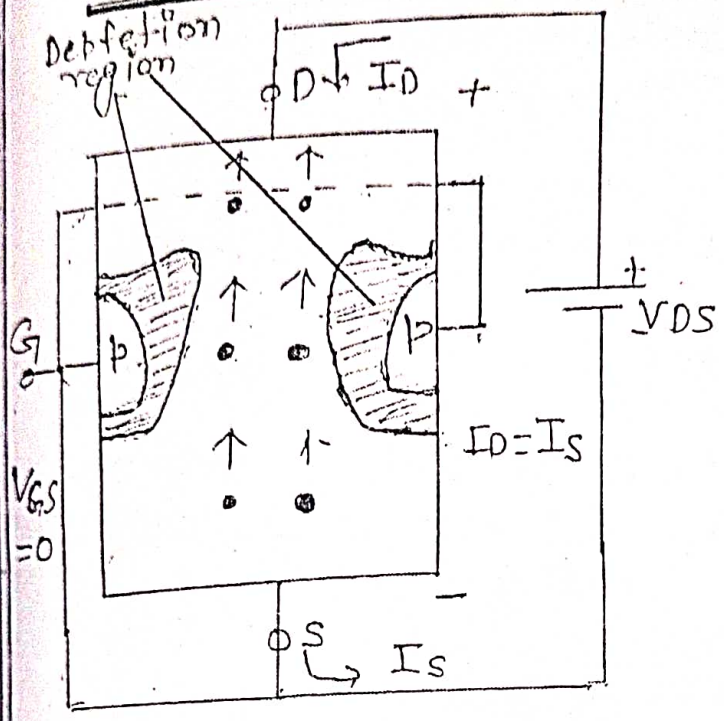
**Ans:-** **Construction:-** A n channel JFET have n type base. On both side of base two heavily doped p regions are formed. So two p-n junction is formed, which are internally connected by a gate terminal. Other two terminal are drain and source.

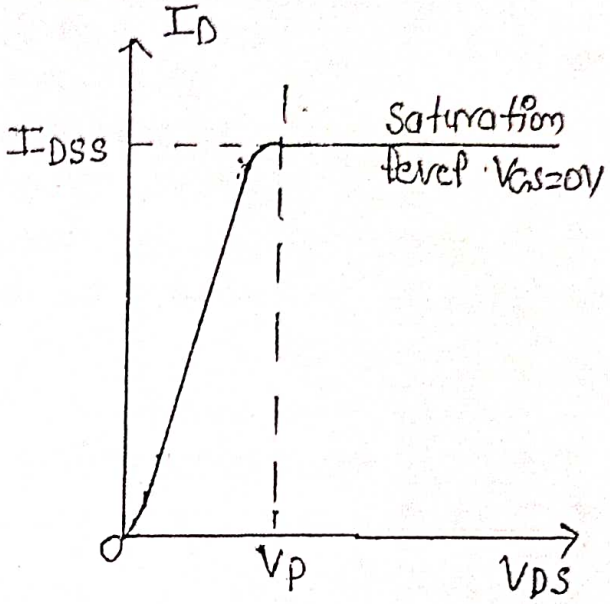



n-Channel JFET

**Operation:-** (i) $V_{DS}$ = positive (>0) (ii) $V_{GS} = 0$

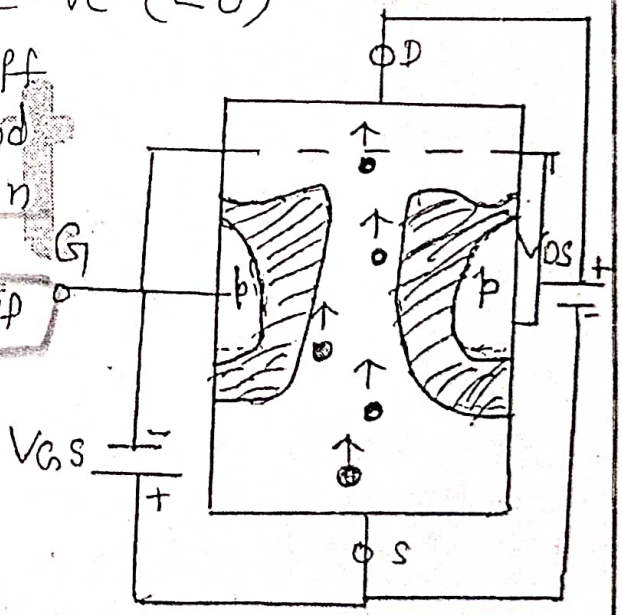
- When $V_{DS}$ is increased more and more electrons move from source to drain. So current increases and depletion layer also increases. So, channel becomes narrower.
- If $V_{DS}$ is further increased a condition comes when depletion layer just touches each other. This condition is called pinch-off condition.
- The value of $V_{DS}$ which establish this condition is called pinch-off voltage ($V_P$). After pinch-off current becomes constant.




(ii) $V_{DS}$ = +ve (>0) and $V_{GS}$ = -Ve (<0)

- As $V_{GS}$ is increased pinch off condition comes earlier and pinch-off voltage decreases in parabolic manner.
- At $V_{GS} = V_P$ current $I_D$ will be zero.



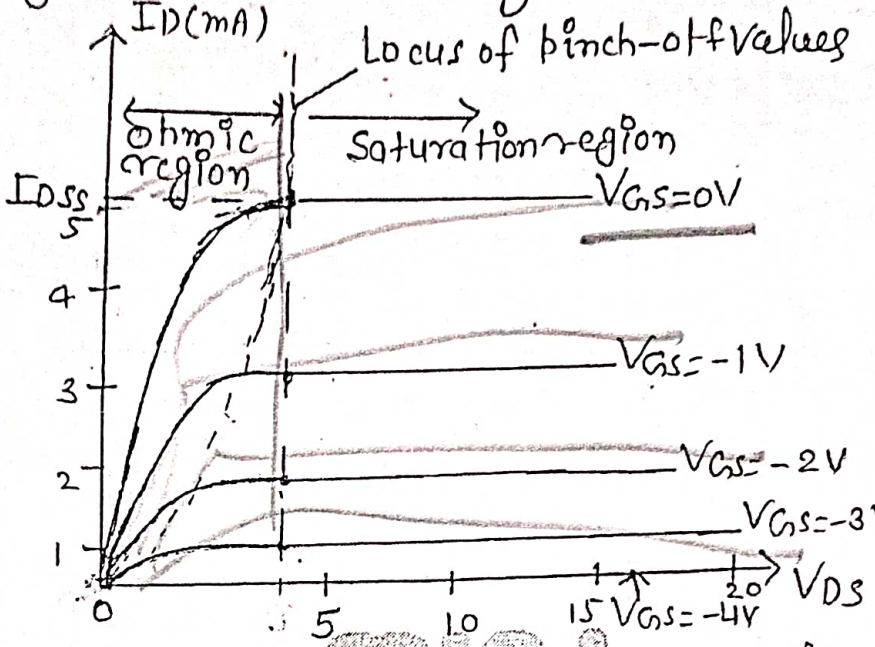

JFET characteristics :-

JFET have two types of characteristics

(i) Drain or output characteristics

(ii) Transfer characteristics

i) Drain or output characteristics :- It is the curve between drain current ($I_D$) and drain to source voltage ($V_{DS}$) while gate to source voltage ($V_{GS}$) should be constant.




- Ohmic region :- → The current $I_D$ increases linearly with $V_{DS}$
  → In ohmic region the slope of graph is dependent on $V_{GS}$. So FET can be used as voltage controlled resistance in this region
- Saturation region or Active region :-
  → After pinch off condition the drain current constant ($I_{DSS}$) and this region is called saturation region.
  → In this region JFET used as an amplifier.

ii) Transfer characteristics :- It is the graph between drain current ($I_D$) and gate to source voltage ($V_{GS}$) while drain to source voltage ($V_{DS}$) should be constant. $I_D$ & $V_{GS}$ are related by shockley eqn.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

let $I_{DSS} = 8mA$ & $V_p = -4V$

a) $V_{GS} = 0V$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8\left[1 - \frac{0}{-4}\right]^2 = 8mA$$

b) $V_{GS} = -1V$

$$I_D = 8\left(1 - \frac{-1}{-4}\right)^2 = 4.5\ mA$$

c) $V_{GS} = -2V$

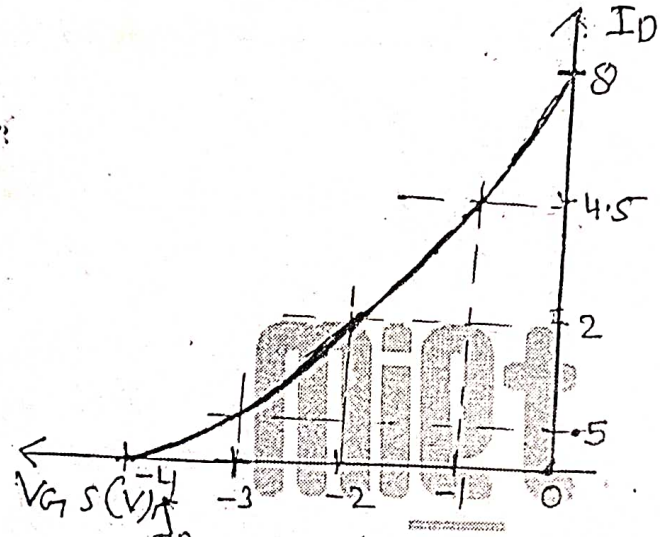
$$I_D = 8\left(1 - \frac{-2}{-4}\right)^2 = 2mA$$

d) $V_{GS} = -3V$

$$I_D = 8\left(1 - \frac{-3}{-4}\right)^2 = 0.5mA$$

e) $V_{GS} = -4V$

$$I_D = 8\left(1 - \frac{-4}{-4}\right)^2 = 0mA$$




$I_D = 0mA$, $V_{GS} = V_p$

Transfer characteristics

**Ques 1** :- Explain how FET can be used as voltage variable resistor. (2017-18, 2016-17, 2015-16)

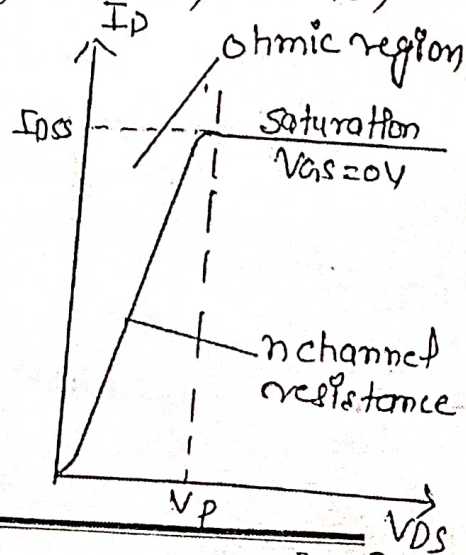
**Ans** :- JFET works a voltage variable resistance (VVR) in ohmic region. The resistance of JFET is given by

$$r_d = \frac{r_o}{\left[1 - \frac{V_{GS}}{V_p}\right]^2}$$

Where $r_o = 10K\Omega$ (Resistance at $V_{GS} = 0$)

a) At $V_{GS} = 0$

$$r_d = \frac{10}{\left[1 - \frac{0}{-4}\right]^2} = 10K\Omega$$



(ii) At $V_{GS} = -2$

$$r_d = \frac{10}{\left(1 - \frac{-2}{-4}\right)^2} = 13.33 K\Omega$$

So JFET works as variable resistance or voltage-controlled resistance in ohmic region.

Q.2 Discuss the various FET parameters and derive relation between them.

Ans (i) AC drain resistance: It is the ratio of change in drain to source voltage ($\Delta V_{DS}$) and change in drain current ($\Delta I_D$) at constant $V_{GS}$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS} = \text{constant}}$$

(ii) Trans conductance ($g_m$): It is the ratio of change in drain current ($\Delta I_D$) and change in gate to source voltage ($\Delta V_{GS}$) at constant drain to source voltage ($V_{DS}$)

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} = \text{constant}}$$

$$= \frac{dI_D}{dV_{DS}}$$

Unit of $g_m$ is Siemen.

(iii) Amplification factor ($\mu$): It is ratio of change in drain to source voltage ($\Delta V_{DS}$) and change in gate to source voltage ($\Delta V_{GS}$) at constant drain current ($I_D$)

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Big| \text{at constant } I_D$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\Rightarrow \boxed{\mu = g_m \times r_d}$$

Ques 3 :- show that transconductance $g_m$ of JFET is related to drain current $I_D$ by

$$g_m = \frac{2}{V_P}\sqrt{I_{DSS} \cdot I_D}$$

Ans :- from Shockley eqn.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \quad \text{---- (1)}$$

diff. eqn 1 w.r.t. $V_{GS}$

$$\frac{dI_D}{dV_{GS}} = I_{DSS} \times 2\left[1 - \frac{V_{GS}}{V_P}\right] \times -\frac{1}{V_P}$$

But $g_m = \frac{dI_D}{dV_{GS}}$

$$\boxed{g_m = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)} \quad \text{---- (2)}$$

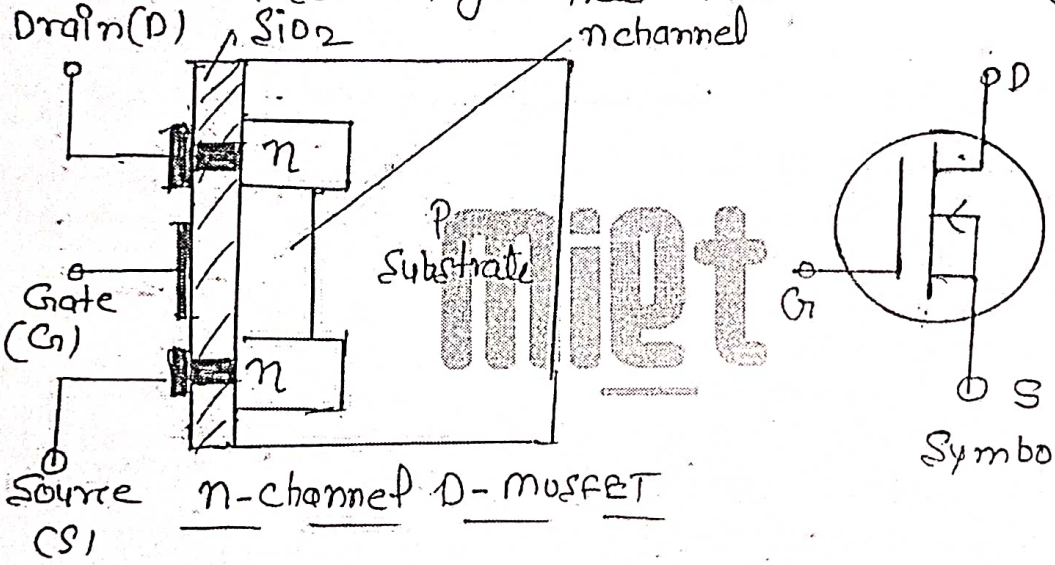
From eqn 1 $\quad 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \quad \text{---- (3)}$

Using 2 and 3 $\quad g_m = -\frac{2I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}}$

$$\boxed{g_m = -\frac{2}{V_P}\sqrt{I_{DSS} \cdot I_D}}$$

Ques 1 :- Explain the construction and working of n-channel depletion type MOSFET. Also draw its drain and transfer characteristics. (2011-12, 2013-14, 2014-15, 2015-16, 2020-21)

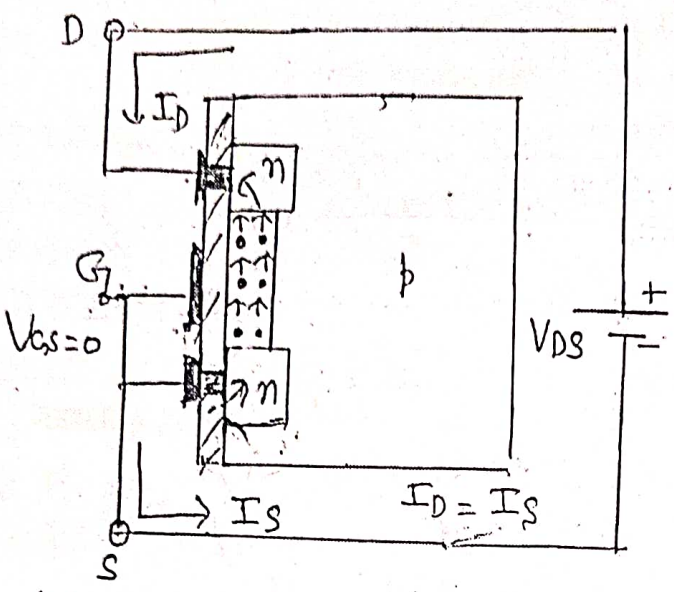
Ans :- construction :- n channel depletion type MOSFET has p type base (substrate). Then two n region are formed. A thin layer of $SiO_2$ (silicon dioxide) is deposited. Drain and source are connected with metalic contact. A n-channel is formed between two n regions. Gate is insulated from n channel by $SiO_2$ (insulator). So $I_G$ is zero. It is also called insulated gate field effect transistor (IGFET)

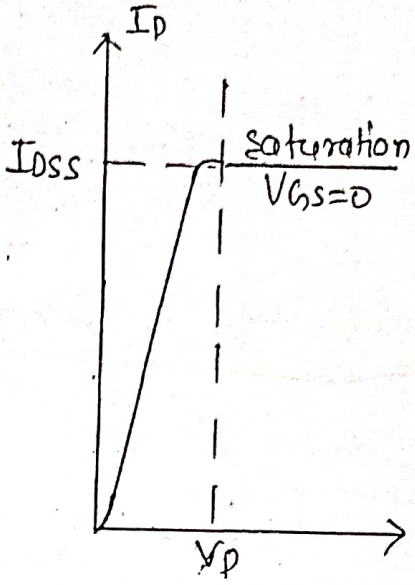



n-channel D-MOSFET

Operation :- (1) $V_{GS} = 0$, $V_{DS} = +ve$ (>0)

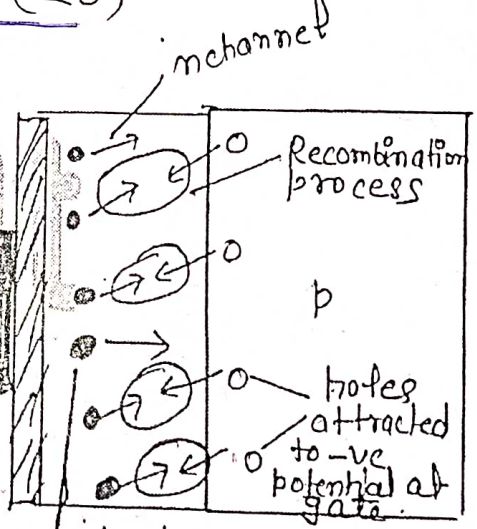
- When $V_{DS}$ is increases more and more electrons move from source to drain. So current increases A condition come when current become constant.
- This condition is called pinch-off condition. the value of $V_{DS}$ which established this condition is called pinch off voltage ($V_P$). After pinch-off current becomes constant.




ii) $V_{DS}$ = +ve (>0), $V_{GS}$ = −ve (<0)

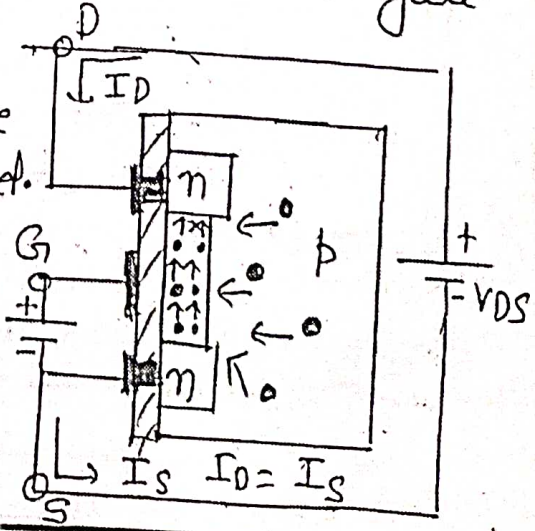
- If $V_{GS}$ is increased then holes in p type substrate move towards the channel.
- So, recombination process occurs in channel.
- So, pinch-off condition comes earlier and pinch-off voltage decreases in parabolic manner. This is called depletion mode.




Electrons repelled by −ve potential at gate.

(iii) $V_{DS}$ = +ve (>0) and $V_{GS}$ = +ve (>0)

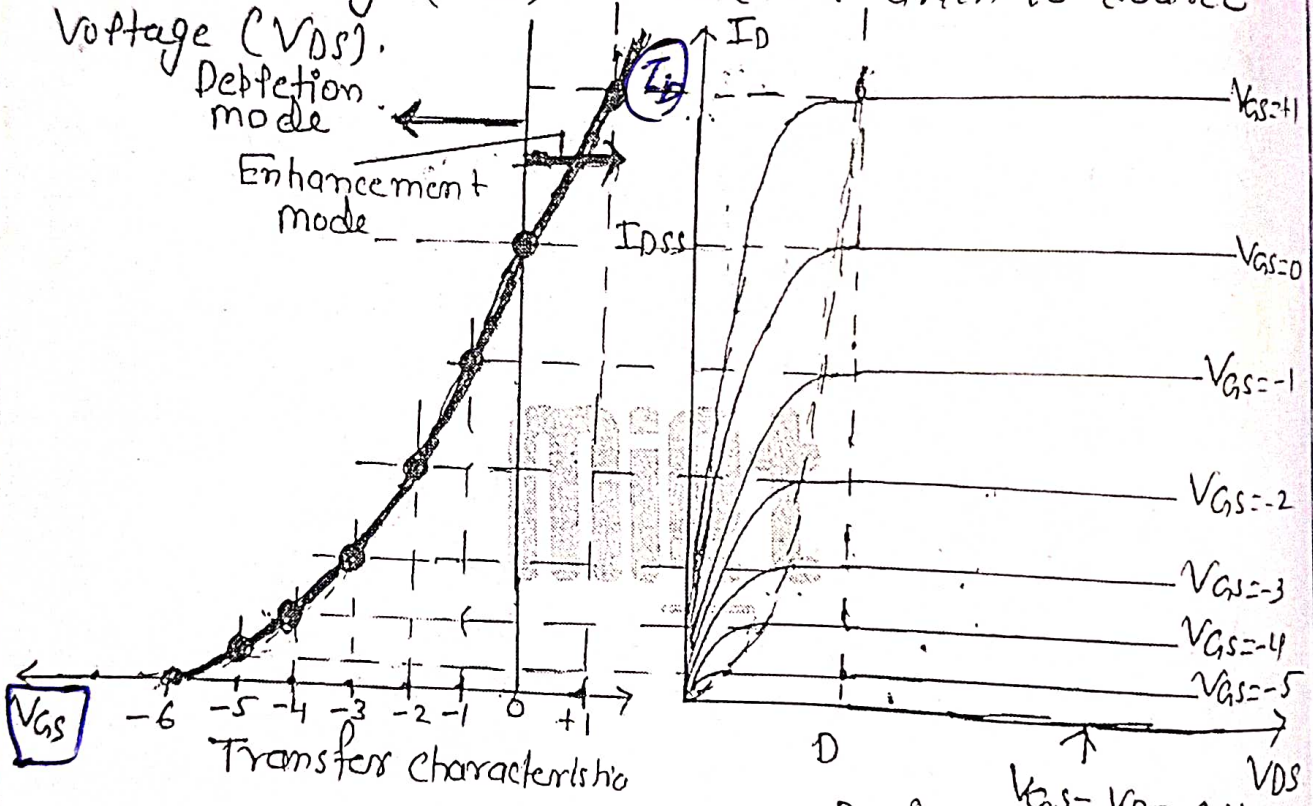
- If positive voltage is applied at gate then electrons in p type substrate move towards the channel.
- So number of electrons in channel increases. So current $V_{GS}$ increases. This is called enhancement mode.



Characteristics :- It has two types of characteristics

i) Drain or output characteristics :- It is the curve between drain current ($I_D$) and drain to source voltage ($V_{DS}$) at constant gate to source voltage ($V_{GS}$).

ii) Transfer characteristics :- It is the curve between drain current ($I_D$) and gate to source voltage ($V_{GS}$) at constant drain to source voltage ($V_{DS}$).



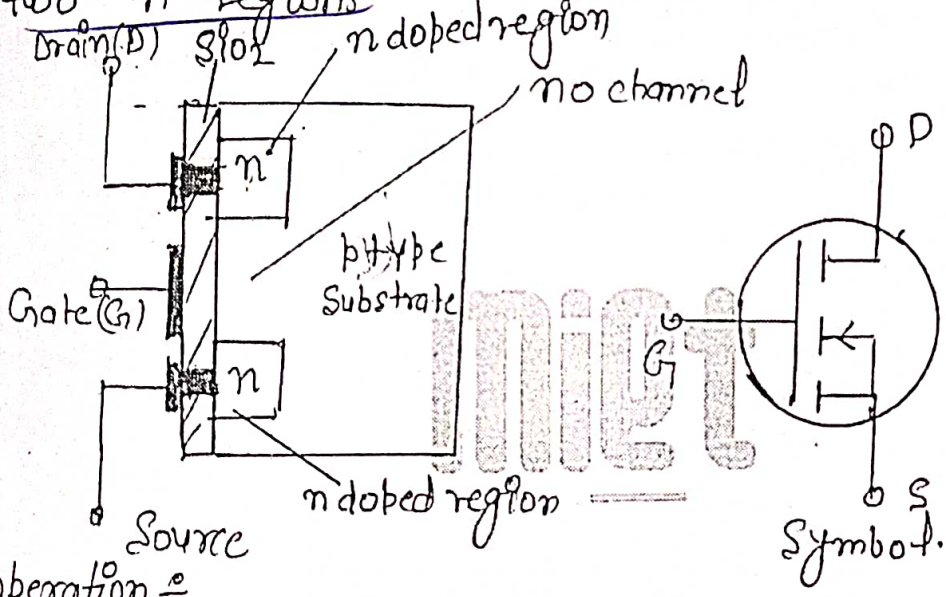

Transfer characteristics

Drain characteristics

Output

Ques:-1 Describe the construction working of enchance-ment MOSFET. Draw drain & Transfer characteristics. (2009-10, 2011-12, 2012-13, 2013-14, 2015-16, 2020-21)

Ans. Construction:- n channel Enhancement MOSFET has p type substrate. In p type substrate two n regions are formed. A ~~thin layer of $SiO_2$~~ (Silicon di oxide) is deposited. Drain and source are connected with the help of metallic contact. There is no channel between two n regions.

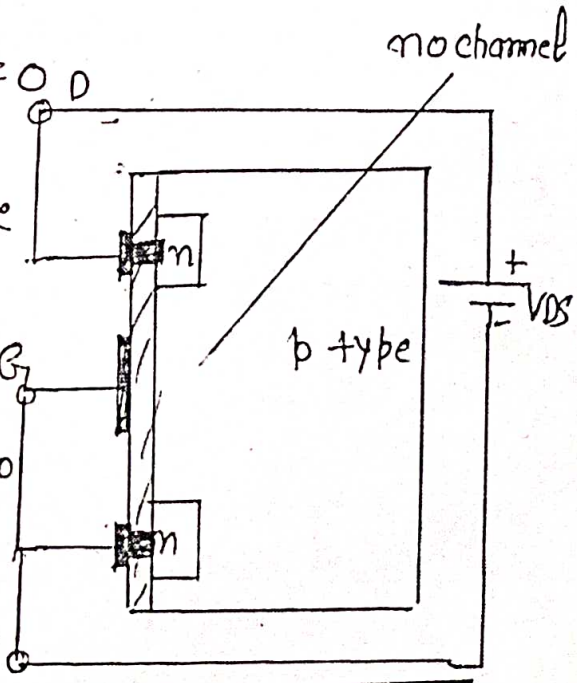



Operation :-

(i) $V_{DS}$ = +ve (>0) and $V_{GS}$ = 0

If $V_{DS}$ is increases then no current will flow because there is no channel.

i.e $I_D = 0$

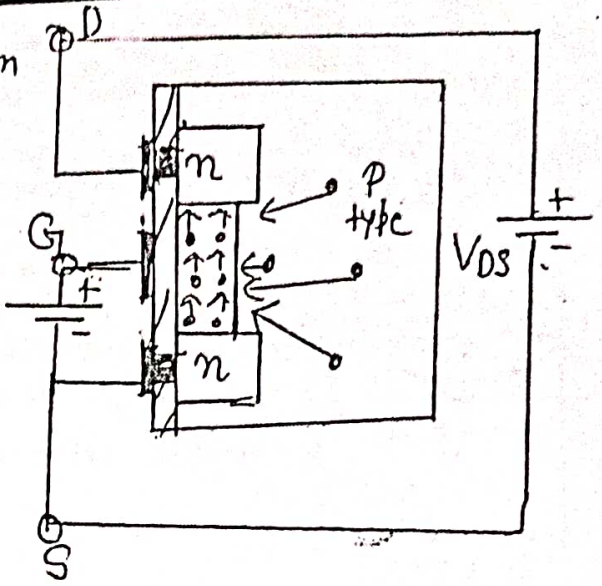



(ii) $V_{DS}$ = +ve (>0) and $V_{GS}$ = +ve (>0)

- If positive gate voltage is applied at gate then electron in p type move towards S

the gate and holes move away from the gate.

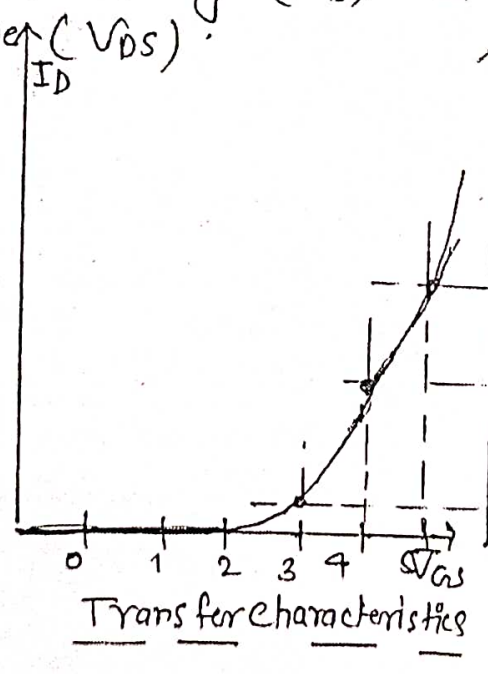
- Till 2V no channel is formed. But after 2V channel is formed.
- This 2V is called threshold voltage ($V_T$). If $V_{GS}$ is further increase then $I_D$ continuosly increases. This is called enhancement MOSFET.



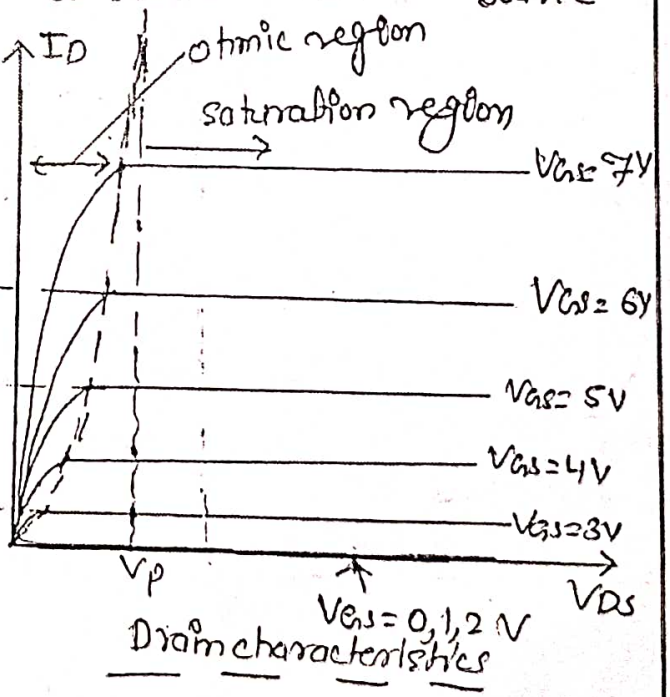

Characteristics :- It has two types of characteristics.

(i) Drain or output characteristics :- It is the curve between drain current ($I_D$) and drain to source voltage ($V_{DS}$) at constant gate to source voltage ($V_{GS}$).

(ii) Transfer characteristics :- It is the curve between drain current ($I_D$) and gate to source voltage ($V_{GS}$) at constant drain to source voltage ($V_{DS}$).




Transfer characteristics




Drain characteristics

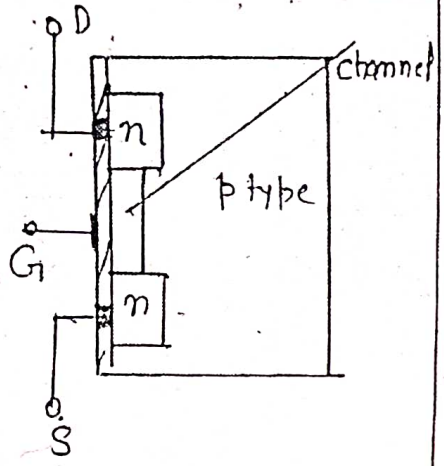
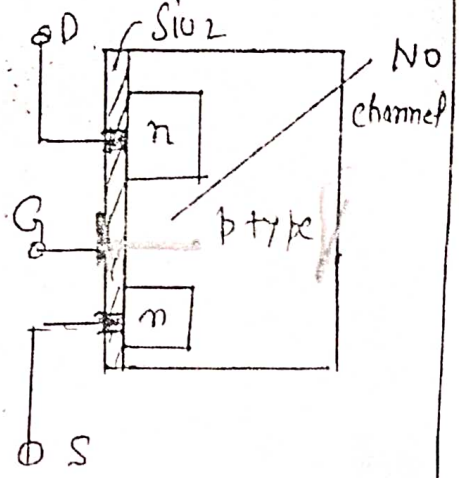
**Ques:- 1** List the difference between JFET & BJT. (2008-09, 2012-13, 2020-21)

**Ans:-** Difference between JFET & BJT

| S.N. | JFET | BJT |
|---|---|---|
| 1. | It is unipolar device i.e. operation depends only on majority carrier. | It is bipolar device i.e. operation depends on majority and minority carrier both. |
| 2. | Voltage controlled device i.e. output is controlled by voltage | current controlled device i.e. output is controlled by current |
| 3. | Input impedance is very high. | Input impedance is very low. |
| 4. | Temperature independent due to absense of of minority carrier | Temperature dependent due to presence of minority carrier |
| 5. | Power consumption is low | power consumption is high. |
| 6. | more cost | less cost |
| 7. | Less noisy | more Noisy |

Ques :- 2 List the difference between D-MOSFET & E- MOSFET.

Ans :- difference between D-MOSFET & E MOSFET

| S.N. | D | E |
|---|---|---|
| 1. |   |   |
| 2. | In D MOSFET channel is present | In E mosfet channel is not present |
| 3. | It works in depletion and Enhancement mode both. | It works in enhancement mode only. |
| 4. | $SiO_2$ layer is between gate and channel | $SiO_2$ layer is between gate and substrate. |
| 5. | No threshold voltage | Threshold voltage exist. |

Ques :- 3 In JFET $I_{DSS}$ = 8mA, $V_p$ = -4 biased at $V_{GS}$ = -1 V. Determine value of $g_m$. (2015-16)

Sol$^n$ :- Give $I_{DSS}$ = 8mA, $V_p$ = -4 V, $V_{GS}$ = -1.8V

$$g_m = \frac{2I_{DSS}}{|V_p|}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$= \frac{2 \times 8}{4}\left[1 - \frac{(-1.8)}{(-4)}\right]$$

$$= 2.2 \text{ mS}$$

# 5 Year's

# University Paper Questions

# (AKTU Question Bank)

# B. Tech I Year [Subject Name: Fund. Of Electronics Engineering]

| 5 Years AKTU University Examination Questions | | Unit-2 | |
|---|---|---|---|
| S. No | Questions | Session | Lecture No |
| 1 | Describe the construction of npn BJT? | 2020-21 | 18 |
| 2 | Explain why BJT is Bipolar Device? | 2015-16 | 18 |
| 3 | Discuss Doping profile and physical appearance of Emitter, base and collector of a transistor? | 2013-14 | 18 |
| 4 | Thickness of base is typically smaller than emitter and collector. Why? | 2011-12 | 18 |
| 5 | Transistor is in saturation when _____? | 2010-11 | 18 |
| 6 | Draw the I/P and O/P characteristics of Common Base Configuration? | 2015-16, 2011-12 | 19 |
| 7 | Draw the I/P and O/P characteristics of Common Emitter Configuration? | 2020-21,2015-16,2011-12,2010-11 | 20 |
| 8 | What is Base Width Modulation? How it affects the characteristics of CB and CE configuration? | 2011-12 | 20 |
| 9 | Explain the Common Collector Configuration in case of npn Transistor? | 2015-16 | 21 |
| 10 | How a transistor can be defined as a Current operated Device? | 2013-14 | 21 |
| 11 | Derive the relationship $I_c = \beta I_b + I_{cbo}$ ? | 2013-14 | 21 |
| 12 | A transistor having $\alpha = 0.975$ and $I_{co} = 10\mu A$ is operated in CE mode. What is $\beta$ for this configuration? If the $I_b$ is $250\mu A$ then calculate $I_e$ and $I_c$? | 2013-14 | 21 |
| 13 | A npn transistor having $\alpha = 0.98$ and $I_{co} = 10\mu A$ is operated in CB mode. If the $I_e$ is 3 mA then calculate $I_b$ and $I_c$? | 2010-11 | 21 |
| 14 | The $\alpha$ and $\beta$ of a transistor are 0.99 and 99 .if its $I_{cbo}$ is 0.1A then $I_{ceo}$ is _____? | 2009-10 | 21 |
| 15 | Derive the relationship between $\alpha$ and $\beta$? | 2011-12 | 21 |
| 16 | Determine $I_e$ ,$\alpha$ and $\beta$ of CB transistor when $I_c = 7ma$, $I_b = 0.1$ mA? | 2011-12 | 21 |
| 17 | How electric field in FET controls a drain Current? | 2013-14 | 22 |
| 18 | What is Pinch off Condition in FET? | 2011-12 | 22 |
| 19 | Explain Ohmic region of JFET? | 2015-16 | 22 |
| 20 | Explain the working of N channel JFET? | 2009-10 | 22 |
| 21 | Explain the Construction and characteristics of JFET? | 2008-09 | 22 |
| 2 | Explain the Characteristics, Working and Construction of P channel Enhancement type Mosfet? | 2015-16,2014-15 | 23 |
| 23 | Explain why FET is Voltage Variable resistor? | 2015-16,2014-15 | 23 |
| 24 | Explain the Transconductance curve of JFET? | 2015-16 | 23 |
| 25 | In JFET $I_{dss} = 6mA$, $V_p = -3V$ biased at $V_{gs} = -2V$ . Determine the value of transconductance? | 2015-16 | 23 |
| 26 | In JFET $I_{dss} = 8mA$, $V_p = -4V$ biased at $V_{gs} = -1.8V$ . Determine the value of transconductance? | 2015-16 | 23 |

| | | | |
|---|---|---|---|
| 27 | Define Ohmic Region, gate cut-off voltage and transconductance in JFET? | 2012-13 | 23 |
| 28 | Given Idss= 9mA and Vp=-3.5V determine Id when Vgs=0V and Vgs=-2V? | 2011-12 | 23 |
| 29 | In JFET Idss=6mA, Vp=-4.5V biased at Vgs= -1.8V , Determine Id at Vgs=-2V and -3.6 V? | 2011-12 | 23 |
| 30 | Why JFET is called Voltage Controlled device ? Draw its structure and O/P characteristics of P channel JFET indicate different regions and its significance? | 2010-11 | 23 |
| 31 | Define: Idss , Pinch off Voltage, Voltage controlled resistance of JFET? | 2009-10 | 23 |
| 32 | Explain the Characteristics, Working and Construction of n Channel Depletion type Mosfet? | 2021-22, 2020-21, 2015-16, 2014-15, 2013-14, 2011-12 | 24 |
| 33 | Explain the working operation of Enhancement and Depletion mode mosfet? And derive the expression of transconductance? | 2020-21,2015-16,2013-14, 2012-13,2011-12,2009-10 | 25 |
| 34 | Explain the Characteristics, Working and Construction of p Channel Depletion type MOSFET? | 2009-10 | 25 |
| 35 | Explain the construction, working and characteristics of MOSFET? | 2008-09 | 25 |
| 36 | List the Differences between JFET and BJT? | 2020-21,2012-13,2008-09 | 26 |
| 37 | Explain Why BJT's are called Bipolar and FET's are Unipolar? | 2011-12, 2009-10 | 26 |
| 38 | What are the advantages of FET over BJT? Define Pinch off Voltage and Drain Resistance of FET? | 2011-12 | 26 |
| 39 | List the differences between JFET and MOSFET? | 2011-12 | 26 |
| 40 | Determine $\beta$ , if IE = 5 mA, IC = 4.95 mA. | 2021-22(O) | |
| 41 | Define transconductance of JFET. | 2021-22(O) | |
| 42 | Differentiate the BJT and JFET. | 2021-22(O), 2021-22(E) | |
| 43 | Describe the construction and working of a NPN transistor in CE configuration with respect to size and doping. Also, draw the input and output characteristic graph. | 2021-22(O) | |
| 44 | Define $\alpha$ and $\beta$ with respect to BJT and derive the relationship between them. A transistor having $\alpha$ = 0.975 and reverse saturation current $I_{CBO}$= 10$\mu$A is operated in CE mode. If the base current is 250$\mu$A. Calculate $I_E$ and $I_C$. | 2021-22(O) | |
| 45 | Determine $\beta_{dc}$ and $I_{CBO}$, If $I_E$ = 6mA, $I_C$ = 5.92mA and $I_{CEO}$=200mA. | 2021-22(E) | |
| 46 | Draw and explain common base N-P-N Transistor with its input and output characteristic graph. Also write an expression for output current. | 2021-22(E) | |
| 47 | Explain the working of enhancement type MOSFET along with their transfer characteristics. | 2021-22(E) | |
| 48 | Describe the construction and working of P-Channel Depletion MOSFET, with characteristic graph. Also Justify that it is a voltage controlled device. | 2021-22(E) | |